REMARKS

Claims 21-23 and 44 are pending in the present application. Claim 21 has been amended. Claim 44 has been presented herewith. Claim 43 has been canceled.

Claim Rejections-35 U.S.C. 103

Claims 21-23 and 43 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Kurihara reference (Japanese Patent Publication No. 2000-030492) in view of the Lee et al. reference (U.S. Patent No. 5,661,685) and the Ozaki reference (U.S. Patent No. 5,337,321), for the same reasons as set forth in the previous Office Action dated January 27, 2005. This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The semiconductor device of claim 21 having an access time measuring test mode features in combination that the fourth signal path "has provided therein a first selector, responsive to a mode of a selection signal, that selectively supplies a prescribed signal or said test clock directly to said fourth pad, a first wiring that directly connects said clock input terminal of said circuit block to an input terminal of said first selector, and a second wiring that directly connects an output terminal of said first selector to said fourth pad", and that the third signal path "has provided therein a second selector which during a normal operation supplies a second prescribed signal other than said test output signal to said third pad and which during a test operation supplies said test output signal to said third pad, a third wiring that directly connects

said signal output terminal of said circuit block to an input terminal of said second selector, and a fourth wiring that directly connects an output terminal of said second selector to said third pad". As further featured, "said third and fourth signal paths are provided so that a difference of timings from when said test clock is output at said fourth pad to when said test output signal is output at said third pad is indicative of an access time of said circuit block". Applicant respectfully submits that these features would not have been obvious in view of the prior art as relied upon by the Examiner for at least the following reasons.

As noted above, the semiconductor device of claim 21 has a fourth signal path which has only first and second wirings and a first selector, and a third signal path which has only third and fourth wirings and a second selector. In other words, only wirings and the first selector are allocated between the clock input terminal of the circuit block and the fourth pad, and only wirings and the second selector are allocated between the signal output terminal of the circuit block and the fourth pad. Clearly, the Kurihara reference as relied upon by the Examiner fails to disclose these features, because the signal path in Fig. 1 of the Kurihara reference interpreted by the Examiner as the third signal path includes flip flop 2, and the signal path in Fig. 1 of the Kurihara reference interpreted by the Examiner as the fourth signal path includes both selector 3 and delay circuit 4.

Claim 21 further features that wiring delay time of the third and fourth signal paths are substantially equal. Therefore, in claim 21 the difference of timings from

when the fourth pad outputs the test clock to when the third pad outputs the test output signal is indicative of an access time of the circuit block. Consequently, the semiconductor device of claim 21 can provide measurement of an access time of the circuit block exactly and easily.

The semiconductor device of the Kurihara reference as relied upon by the Examiner has a signal path which connects a clock input terminal of a circuit block (memory circuit 1 in Fig. 1) and pad TCK, and a signal path which connects a signal output terminal of circuit block 1 and pad TD0. However, the semiconductor device in Fig. 1 of the Kurihara reference as relied upon by the Examiner has delay circuit 4 between the clock input terminal and pad TCK, and also has flip-flop circuit 2 between the signal output terminal of circuit block 1 and pad TD0. Therefore, wiring delay time of these paths are not equal, because delay circuit 4 and flip-flop 2 are arranged along these paths. Consequently, the difference of timings from when a test clock is output at pad TCK in Fig. 1 of the Kurihara reference to when a test output signal is output at pad TD0 in Fig. 1 of the Kurihara reference is not indicative of an access time of circuit block 1.

As described in paragraphs [0021] and [0027] of the English translation of the Kurihara reference, the circuit measures the access time of circuit block 1 by detecting a delay condition in which flip-flop circuit 2 can hold the output data of circuit block 1. Because of this, plural measuring processes which include changing the delay amount of the delay circuit are necessary. Therefore, flip-flop circuit 2 and delay circuit 4 are

indispensable elements of the Fig. 1 device of the Kurihara reference. In contrast, the third and fourth signal paths of claim 21 do not comprise a flip-flop circuit and a delay circuit, because it is necessary that the delay times of the third and fourth signal paths be substantially the same. Consequently, it should be understood that while the purpose of the Kurihara reference may be the same as that of the present invention, the constitution and principles of the Kurihara reference are not the same as featured in claim 21.

The Ozaki reference as relied upon by the Examiner discloses a circuit which includes a combination of flip-flop circuits and selectors. However, the Ozaki reference as relied upon by the Examiner fails to disclose signal paths provided so that a difference of timings from when a test clock is output at a fourth pad to when a test output signal is output at a third pad is indicative of an access time of a circuit block. Similarly, the Lee et al. reference as relied upon by the Examiner fails to disclose these features.

Applicant thus respectfully submits that the Ozaki and Lee et al. references as secondarily relied on by the Examiner do not overcome the above noted deficiencies of the primarily relied upon Kurihara reference. Applicant further respectfully submits that the semiconductor device of claim 21 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection, insofar as it may pertain to the claims 21-23, is improper for at least these reasons.

Claim 44

Applicant respectfully submits that claim 44 would not have been obvious in view of the prior art as relied upon by the Examiner at least by virtue of dependency upon claim 21 for the reasons as set forth above, and by further reason of the features therein.

Conclusion

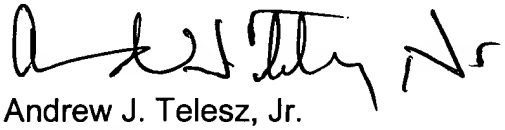
The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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